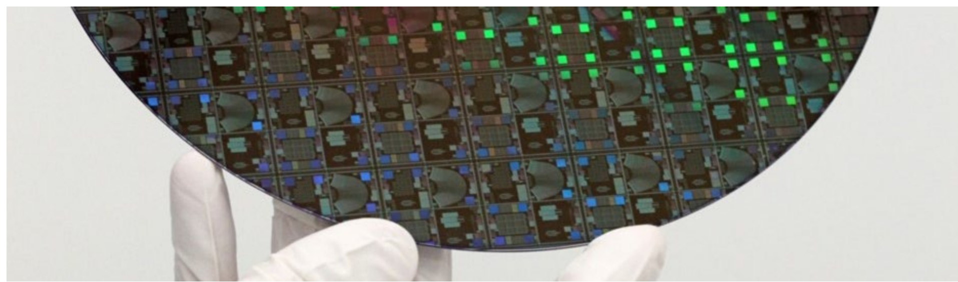


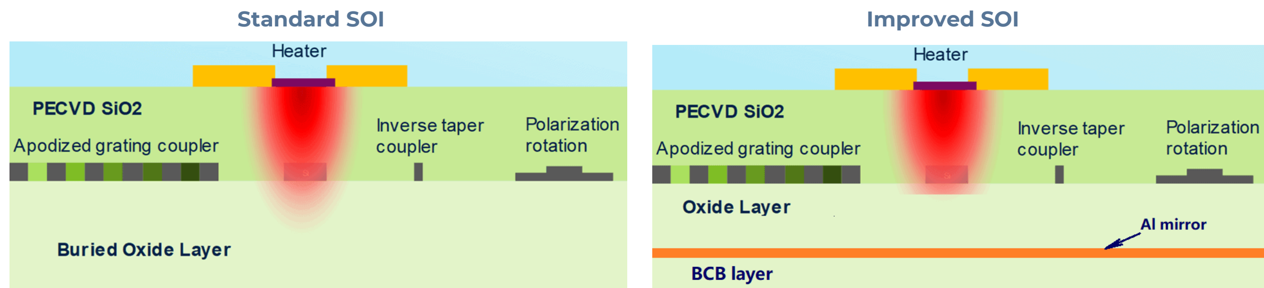
Prototyping manual

This manual describes the prototyping options currently offered by SiPhotonIC.

SiPhotonIC SOI platforms

Standard SOI platforms

SiPhotonIC offers currently two verified SOI platforms for fast prototyping, the **Standard SOI** and the **Improved SOI**. Both have 220nm and 250nm PDK libraries, with the 250nm PDK library being more mature. The **Standard SOI** can be typically used for optical communications, sensing and other generic applications, while the **Improved SOI** (<1dB coupling) can be used for applications where coupling loss is critical, such as quantum photonics.



Custom components/stacks/processes

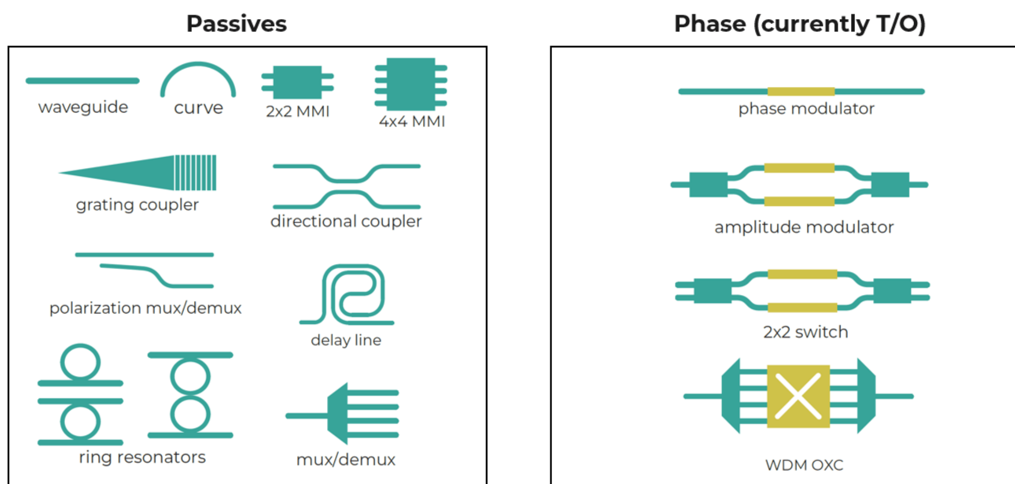
SiPhotonIC also allows you to submit an order with:

- **custom-designed components** based on the platforms' generic specifications (220nm / 250nm SOI)
- **custom stacks** with the materials and layers of choice
- **custom processes** on your provided chips/wafers or part of your fabrication procedure

Layout design options

SiPhotonIC gives you design flexibility by supporting the following PDKs for its standard components:

- SYNOPSYS OptoDesigner
- LUCEDA IPKISS
- GDSII GDS libraries to use with L-edit IC, Nazca, GDS Factory etc.



SiPhotonIC TECHNOLOGIES

SiPhotonIC Technologies ApS
Virum Stationsvej 207, 2830 Virum, Denmark
Tel: +45 50 17 86 66 info@siphotonic.com www.siphotonic.com

Prototyping options

1) EBL lithography prototyping (standard)

SiPhotonIC offers EBL lithography for taping out designs that require high-resolution (>20nm) for their structures. The fabrication starts **immediately** after the receipt of the final design mask.

This service is offered for orders of:

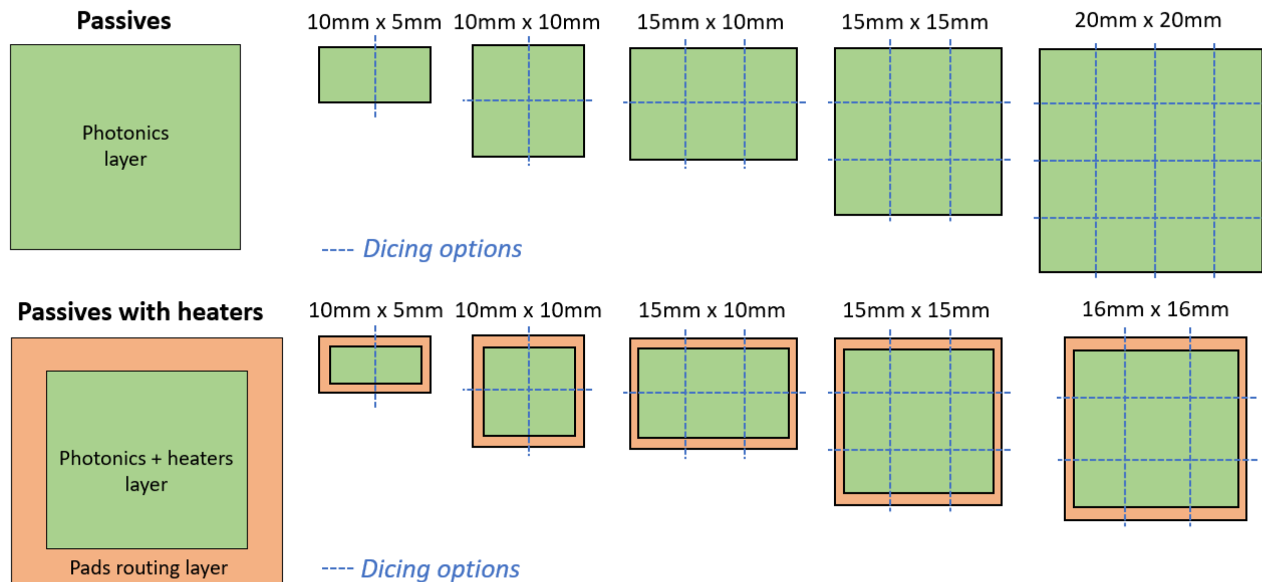
- **1-10 SOI samples (chips)**

For the standard EBL service, the customer needs to choose from the following checklist:

(include your options in your email request)

- **SOI Platform:** Standard SOI ☐, Improved SOI ☐
- **Top Si thickness:** 220nm SOI ☐, 250nm SOI ☐
- **Functionality:** Passives ☐, Passives with heaters ☐
- **Cladding:** Air top ☐, SiO2 top ☐, Other cladding (polymer etc.) ☐
- **Bottom Oxide (BOX) thickness = _____ , Top Oxide (TOX) thickness = ____**
- **Etching depth:** Full-etching ☐, Shallow-etching at ____ nm ☐, Multiple etching depths = at _____ nm ☐
- **Dicing options:**
  - Saw dicing: ☐ in __ samples *(minimum dicing in 5mm x 5mm chips)*
  - Stealth dicing ☐ in __samples *(for PICs with edge couplers)*
- **Design area:** __mm × __ mm *(Choose from below. The minimum design area for ordering is 10mm x 5mm)*

Standard design areas for EBL



Delivery times for EBL

For standard processing, the delivery times (shipping) are:

Process	Delivery time (standard cycle)	Rapid cycle premium
Standard SOI - Passives	1.5 month FRO	1 month FRO
Standard SOI – Passives & heaters	2.5 months FRO	2 months FRO
Improved SOI - Passives	2.5 months FRO	2 months FRO
Improved SOI – Passives & heaters	3.5 months FRO	3 months FRO
Custom	Contact us	

Custom processes may affect the number & sizes of the samples

For stealth dicing (edge couplers), the shipping time increases by 2 weeks.

For Rapid Cycle Premium, we follow a "pay-the-extra-only-if-we-ship" policy. This means that you will finally pay the Premium price only if we ship within the given Premium time, otherwise you will pay the respective Standard price of the category.

2) DUV lithography prototyping (standard)

SiPhotonIC offers **"DUV-on-demand" lithography** for taping out designs that require >200nm resolution for their structures, in small and medium volumes. The fabrication starts **immediately** after the receipt of the final design mask.

This service is offered for orders of:

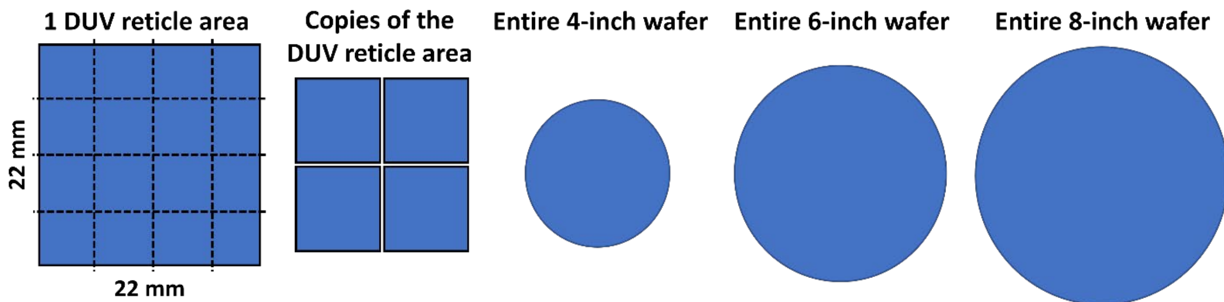
- **design area = 1 DUV reticle.** You book the entire area of our DUV reticle (22mm x 22mm, excl. our DUV markers) that you can allocate for your chip designs. You may decide to go for :
  - **1 exposure** of this design area
  - **multiple exposures** of this design area
- **entire 4'', 6'' and 8'' wafers** (whole wafers or diced into samples of choice)

For the **"DUV-on-demand"** service, the customer needs to choose from the following checklist:

(include your options in your email request)

- **SOI Platform:** Standard SOI ☐, Improved SOI ☐
- **Top Si thickness:** 220nm SOI ☐, 250nm SOI ☐
- **Functionality:** Passives ☐, Passives with heaters ☐
- **Cladding:** Air top ☐, SiO2 top ☐, Other cladding (polymer etc.) ☐
- **Etching depth:** Full-etching ☐, Shallow-etching at ____ nm ☐, Multiple etching depths = at _____ nm ☐
- **Dicing options:**
  - Saw dicing: ☐ in __ samples *(minimum dicing in 5mm x 5mm chips)*
  - Stealth dicing ☐ in __samples *(for PICs with edge couplers)*
- **Design area:** _____ *(Choose from below. The minimum design area for ordering is 1 DUV reticle area)*

Standard design areas for DUV-on-demand



Delivery times for DUV-on-demand

For standard processing, the delivery times (shipping) are:

Process	Delivery time (standard cycle)	Rapid cycle premium
Standard SOI - Passives	1.5 month FRO	1 month FRO
Standard SOI – Passives & heaters	2.5 months FRO	2 months FRO
Improved SOI - Passives	2.5 months FRO	2 months FRO
Improved SOI – Passives & heaters	3.5 months FRO	3 months FRO
Custom	Contact us	

Custom processes may affect the number & sizes of the samples
For stealth dicing (edge couplers), the shipping time increases by 2 weeks.
For Rapid Cycle Premium, we follow a "pay-the-extra-only-if-we-ship" policy. This means that you will finally pay the Premium price only if we ship within the given Premium time, otherwise you will pay the respective Standard price of the category.

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3) Combined EBL-DUV prototyping (custom)

SiPhotonIC offers the possibility to combine EBL and DUV lithography steps for taping out complex designs in medium volume but also with high-resolution requirements (<20 nm) for only some of their structures.

To consider this option that comprises 2 lithographic techniques, the following need to be taken into consideration:

- the design area that requires EBL resolution should be a small percentage of the total design area
- some part of the design will be sacrificed for additional lithographic markers
- additional waveguide converter structures (small tapers) should be interpolated in the DUV-exposed waveguides and the EBL-exposed waveguides to minimize the effect of the misalignment error of the extra lithographic step(s). SiPhotonIC can provide these converters as building blocks.
- custom integration stacks may require more than 1 DUV and 1 EBL steps, according to the complexity of the fabrications and the materials.

Please, send us to info@siphotonic.com your project requirements and we will suggest the best pathway to integrate it.

4) Custom components/stacks/processes

SiPhotonIC also allows you to prototype photonic ICs with fully customized components, stacks and processes.

- **custom-designed components** based on the platforms' generic specifications (220nm / 250nm SOI)
  You can request our platform specifications and design your own compatible photonic structures that we will fabricate with either standard or custom processes for you. You can decide to use your custom components with any of our PDK components that are missing to complete your circuit.
- **custom stacks** with the materials and layers of choice
  You can submit a sketch of your envisioned or simulated photonic structure or stack and we will let you know the best way and process set to fabricate it. You may choose from all available materials we can process (assuming their compatibility).
- **custom processes** on your provided chips/wafers or part of your fabrication procedure
  If you want to include an entire process or a specific process step for your prototyping project, we can perform this as NRE for you, including the required test runs.

Some examples of non-standard processes & materials on our previous prototypes include:

- SiO_2 (Top oxide) window openings for sensing applications
- Si waveguides under-etching optimization
- multiple stacks of Si-SiN layers
- lithium niobate-on-insulator (LNOI) structures
- graphene structures
- plasmonic structures
- metasurfaces of silicon layer on a sapphire substrates

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